CLAIMS

We claim:

1. A method of fabricating word-line spacers, comprising the steps:

a) providing a substrate having an inchoate split-gate flash memory structure formed thereover;

b) forming a conductive layer over the substrate and the inchoate split-gate flash memory structure; the conductive layer having a upper portion and lower vertical portions over the inchoate split-gate flash memory structure and lower horizontal portions over the substrate;

c) forming a dual-thickness oxide layer over the conductive layer; the dual-thickness oxide layer having a greater thickness over the upper portion of the conductive layer;

d) partially etching-back the oxide layer to remove at least the oxide layer from over the lower horizontal portions of the conductive layer to expose the underlying portions of the conductive layer;

and

e) etching:

i) away the exposed portions of the conductive layer over the substrate; and

ii) through at least a portion of the thinned oxide layer and into the exposed underlying portion of the conductive layer to expose a portion of the inchoate split-gate flash memory structure and

to form the word-line spacers adjacent the inchoate split-gate flash memory structure.

2. The method of claim 1, wherein the substrate is a silicon substrate or a germanium substrate.

3. The method of claim 1, wherein the conductive layer has a thickness of from about 1000 to 2000Å and the word-line spacers each have a thickness of from about 1700 to 1900Å.

4. The method of claim 1, wherein the conductive layer has a thickness of from about 1250 to 1850Å and the word-line spacers each have a thickness of from about 1750 to 1850Å.

5. The method of claim 1, wherein the conductive layer has a thickness of about 1800Å and the word-line spacers each have a thickness of about 1800Å.

6. The method of claim 1, wherein the word-line spacers include upper and lower outer side walls and remnants of the thinned oxide layer remain over the upper, outer side walls of word-line spacers.

7. The method of claim 1, wherein the upper portion of the conductive layer is implanted and the dual-thickness oxide layer is thermally grown over the conductive layer.

8. The method of claim 1, including the steps of:

masking the polysilicon layer to expose the upper portion of the conductive layer before formation of the dual-thickness oxide layer; and

then implanting the exposed upper portion of the conductive layer;

wherein the dual-thickness oxide layer is thermally grown over the partially non-implanted conductive layer.

9. The method of claim 1, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 200 to 2000Å and the remainder of the dual-thickness oxide layer has a thickness of from about 100 to 500Å.

10. The method of claim 1, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 400 to 600Å and the remainder of the dual-thickness oxide layer has a thickness of from about 200 to 400Å.

11. The method of claim 1, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of about 500Å and the remainder of the dual-thickness oxide layer has a thickness of about 250Å.

12. The method of claim 1, wherein the dual-thickness oxide layer is formed having a poor step coverage.

13. The method of claim 1, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 300 to 700Å and the remainder of the dual-thickness oxide layer has a thickness of from about 180 to 420Å.

14. The method of claim 1, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 390 to 610Å and the remainder of the dual-thickness oxide layer has a thickness of from about 250 to 350Å.

15. The method of claim 1, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of about 500Å and the remainder of the dual-thickness oxide layer has a thickness of about 300Å.

16. The method of claim 1, wherein the conductive layer is comprised of polysilicon.

17. The method of claim 1, wherein the partial etching-back of the oxide layer also thins the oxide layer having a greater thickness over the upper portion of the conductive layer.

18. A method of fabricating word-line spacers, comprising the steps:

a) providing a substrate having an inchoate split-gate flash memory structure formed thereover;

b) forming a polysilicon layer over the substrate and the inchoate split-gate flash memory structure; the polysilicon layer having a first upper portion and lower vertical portions over the inchoate split-gate flash memory structure and lower horizontal portions over the substrate;

c) forming an oxide layer over the polysilicon layer; the oxide layer having:

i) a first portion over the first upper portion of the polysilicon layer; the first oxide layer portion having a first thickness; and

ii) second portions over the lower vertical and horizontal portions of the polysilicon layer; the second oxide layer portions each having a second thickness that is less than the first thickness;

d) partially etching-back the oxide layer to:

i) thin the first oxide layer portion over the first upper portion of the polysilicon layer;

ii) remove the horizontal second oxide layer portions from over the lower horizontal portions of the polysilicon layer to expose the horizontal portions of the polysilicon layer over the substrate; and

iii) remove portions of the vertical second oxide layer portions from over the lower vertical portions of the polysilicon layer to expose vertical portions of the polysilicon layer contiguous with the exposed horizontal portions of the polysilicon layer;

and

e) etching:

i) through the horizontal thinned first oxide layer portion to expose a second upper portion of the polysilicon layer thereunder;

ii) away the exposed horizontal portions of the polysilicon layer over the substrate; and

iii) the second upper portion of the polysilicon layer to remove the polysilicon layer over the inchoate split-gate flash memory structure and partially remove the polysilicon layer adjacent the inchoate split-gate fiash memory structure to form the word-line spacers.

19. The method of claim 18, wherein the substrate is a silicon substrate or a germanium substrate.

20. The method of claim 18, wherein polysilicon layer has a thickness of from about 1000 to 2000Å and the word-line spacers each have a thickness of from about 1700 to 1900Å.

21. The method of claim 18, wherein polysilicon layer has a thickness of from about 1250 to 1850Å and the word-line spacers each have a thickness of from about 1750 to 1850Å.

22. The method of claim 18, wherein polysilicon layer has a thickness of about 1800Å and the word-line spacers each have a thickness of about 1800Å.

23. The method of claim 18, wherein the word-line spacers include upper and lower outer side walls and remnants of the thinned oxide layer remain over the upper, outer side walls of word-line spacers.

24. The method of claim 18, wherein the upper portion of the polysilicon layer is implanted and the dual-thickness oxide layer is thermally grown over the polysilicon layer.

25. The method of claim 18, including the steps of:

masking the polysilicon layer to expose the upper portion of the polysilicon layer before formation of the dual-thickness oxide layer; and

then implanting the exposed upper portion of the polysilicon layer;

wherein the dual-thickness oxide layer is thermally grown over the partially non-implanted polysilicon layer.

26. The method of claim 18, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 200 to 2000Å and the remainder of the dual-thickness oxide layer has a thickness of from about 100 to 500Å.

27. The method of claim 18, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 400 to 600Å and the remainder of the dual-thickness oxide layer has a thickness of from about 200 to 400Å.

28. The method of claim 18, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of about 500Å and the remainder of the dual-thickness oxide layer has a thickness of about 250Å.

29. The method of claim 18, wherein the dual-thickness oxide layer is formed having a poor step coverage.

30. The method of claim 18, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 300 to 700Å and the remainder of the dual-thickness oxide layer has a thickness of from about 180 to 420Å.

31. The method of claim 18, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of from about 390 to 610Å and the remainder of the dual-thickness oxide layer has a thickness of from about 250 to 350Å.

32. The method of claim 18, wherein the portion of the dual-thickness oxide layer having a greater thickness has a thickness of about 500Å and the remainder of the dual-thickness oxide layer has a thickness of about 300Å.

33. A split-gate flash memory structure, comprising:

an inchoate split-gate flash memory structure 12 having outer vertical surfaces; and

word-line spacers 30 adjacent the vertical surfaces; the word-line spacers being partially etched-back and having raised upper, outer sidewall portions extending above the inchoate split-gate flash memory structure 12.

34. The structure of claim 33, wherein the word-line spacers 30 are comprised of a conductive material.

35. The structure of claim 33, wherein the word-line spacers 30 are comprised of polysilicon.

36. The structure of claim 33, including an oxide remnant 32 over at least the upper lateral portions of each upper, outer sidewall portion.

37. The structure of claim 33, wherein the word-line spacers 30 each have a width of from about 1700 to 1900Å.

38. The structure of claim 33, wherein the word-line spacers 30 each have a width of from about 1750 to 1850Å.

39. The structure of claim 33, wherein the word-line spacers 30 each have a width of about 1800Å.